ABSTRACT OF THE DISCLOSURE

A fabrication method of a semiconductor device includes forming an interlayer dielectric film over an entire surface of a semiconductor substrate that includes a lower line. A barrier layer having an etching rate that is lower than an etching rate of the interlayer dielectric film is formed on the interlayer dielectric film. The barrier layer is selectively etched to expose a predetermined region of the interlayer dielectric film. Next, a photoresist pattern is formed on the barrier layer having an opening of a predetermined area corresponding to the exposed region of the interlayer dielectric film. The opening of the photoresist pattern has an area that is greater than an area of the exposed region of the interlayer dielectric film. The line opening and the via are then simultaneously formed by etching the exposed regions of the barrier layer and the interlayer dielectric film. Finally, a metal plug is formed by filling the line opening and the via with a metal material.